A2 cncl.

Silicon dioxide 420 is deposited by CVD, or thermally grown, on layer 410. Layers 310, 410, 420 are referenced as 160. Doped polysilicon 170, or some other conductive material, is deposited to provide the control gates (possibly wordlines each of which provides the control gates for a row of memory cells). The layers 170, 420, 410, 310, 110, 130 are patterned as needed. Source/drain regions 140 are formed by doping. Additional layers (not shown) may be formed to provide select gates, erase gates, or other features. See the aforementioned U.S. patent no. 6,355,524 for an exemplary memory fabrication process that can be modified to incorporate the floating gate nitridation described above.

IN THE CLAIMS

A3

1. (Amended) A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first layer comprising a silicon surface, the first layer being to provide one or more floating gates for the nonvolatile memory;

nitriding the silicon surface of the first layer to incorporate nitrogen atoms into said surface, wherein the nitriding operation comprises ion implantation of a material comprising nitrogen into the silicon surface;

forming a first dielectric at the nitrided surface, wherein forming the first dielectric comprises forming silicon oxide at the nitrided surface;

forming a conductive layer separated from the nitrided surface by the first dielectric, the conductive layer providing one or more control gates for the nonvolatile memory.

2. (Unchanged) The method of Claim 1 wherein forming the silicon oxide at the nitrided surface comprises forming the silicon oxide by thermal oxidation.

A4

3. (Amended) The method of Claim 1 wherein the silicon surface of the first layer is a polysilicon surface.

Please cancel Claims 4-6.

A5

7. (Amended) A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

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forming a first layer to provide one or more floating gates for the nonvolatile memory;

forming a first dielectric on a surface of the first layer, wherein the first dielectric comprises a first surface comprising silicon oxide;

nitriding the first surface of the first dielectric to incorporate nitrogen atoms into the first surface, wherein the nitriding operation comprises ion implantation of a material comprising nitrogen into the first surface;

forming a conductive layer on the nitrided first surface of the first dielectric, the conductive layer providing one or more control gates for the nonvolatile memory.

Please cancel Claims 8 and 9.

Please add the following claims.

10. (New) The method of Claim 1 wherein forming the first dielectric comprises:

forming the first dielectric to have a silicon oxide surface; and

nitriding the silicon oxide surface of the first dielectric to incorporate nitrogen atoms into the silicon oxide surface.

11. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface comprises ion implantation of a material comprising nitrogen into the silicon oxide surface.

12. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface comprises generating a plasma comprising ions comprising nitrogen, and exposing the silicon oxide surface to the plasma.

13. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface comprises remote plasma nitridation.

14. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface comprises decoupled plasma nitridation.

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15. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface results in forming at the silicon oxide surface a nitrided silicon oxide layer less than 3 nm thick.

16. (New) The method of Claim 1 wherein the nitriding of the silicon surface results in forming at the silicon surface a layer of nitrided silicon less than 3 nm thick.

17. (New) A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first layer comprising a silicon surface, the first layer being to provide one or more floating gates for the nonvolatile memory;

nitriding the silicon surface of the first layer by remote plasma nitridation and/or decoupled plasma nitridation to incorporate nitrogen atoms into said surface;

forming a first dielectric at the nitrided surface, wherein forming the first dielectric comprises forming silicon oxide at the nitrided surface;

forming a conductive layer separated from the nitrided surface by the first dielectric, the conductive layer providing one or more control gates for the nonvolatile memory.

18. (New) The method of Claim 17 wherein the nitriding operation comprises remote plasma nitridation.

19. (New) The method of Claim 17 wherein the nitriding operation comprises decoupled plasma nitridation.

20. (New) The method of Claim 17 wherein forming the silicon oxide at the nitrided surface comprises forming the silicon oxide by thermal oxidation.

21. (New) The method of Claim 17 wherein the silicon surface of the first layer is a polysilicon surface.

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22. (New) The method of Claim 17 wherein forming the first dielectric comprises:

forming the first dielectric to have a silicon oxide surface; and

nitriding the silicon oxide surface of the first dielectric to incorporate nitrogen atoms into the silicon oxide surface.

23. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface comprises ion implantation of a material comprising nitrogen into the silicon oxide surface.

24. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface comprises generating a plasma comprising ions comprising nitrogen, and exposing the silicon oxide surface to the plasma.

25. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface comprises remote plasma nitridation.

26. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface comprises decoupled plasma nitridation.

27. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface results in forming at the silicon oxide surface a nitrided silicon oxide layer less than 3 nm thick.

28. (New) The method of Claim 17 wherein the nitriding of the silicon surface results in forming at the silicon surface a layer of nitrided silicon less than 3 nm thick.

29. (New) The method of Claim 7 wherein the ion implantation results in forming at the first surface a nitrided silicon oxide layer less than 3 nm thick.

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